IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device package, comprising:

a semiconductor device including at least one bond pad on an active surface thereof and at least one recess in a peripheral edge thereof;

at least one outer connector corresponding to the at least one bond pad, the at least one outer connector positioned ~~on a peripheral edge of the semiconductor device~~ at least partially within the at least one recess and having a height that extends substantially along a height of the peripheral edge; and

at least one conductive trace extending between the at least one bond pad and the at least one outer connector.

2. (Original) The semiconductor device package of claim 1, further comprising:

an insulative layer positioned beneath at least the at least one conductive trace.

3. (Withdrawn) The semiconductor device package of claim 1, further comprising:

an insulative layer positioned over at least the at least one conductive trace and the at least one bond pad.

4. (Original) The semiconductor device package of claim 1, further comprising:

a back side insulative layer substantially covering a back side of the semiconductor device.

5. (Original) The semiconductor device package of claim 1, wherein the at least one outer connector comprises opposite surfaces exposed at the active surface and a back side of the semiconductor device.

6. (Original) The semiconductor device package of claim 5, wherein the at least one outer connector comprises a recess extending substantially from one of the opposite surfaces to another of the opposite surfaces.

7. (Original) The semiconductor device package of claim 6, wherein the recess has a semicylindrical shape.

8. (Original) The semiconductor device package of claim 1, comprising a plurality of outer connectors.

9. (Original) The semiconductor device package of claim 8, comprising a plurality of conductive traces that corresponds to at least some of the plurality of outer connectors.

10. (Original) The semiconductor device package of claim 9, wherein each of the plurality of conductive traces establishes electrical communication between a bond pad of the semiconductor device and a corresponding outer connector of the plurality of outer connectors.

11. (Withdrawn) The semiconductor device package of claim 8, wherein each of the plurality of outer connectors is positioned on a single peripheral edge of the semiconductor device.

12. (Original) The semiconductor device package of claim 8, wherein outer connectors of the plurality of outer connectors are positioned adjacent to at least two peripheral edges of the semiconductor device.

13. (Withdrawn) An intermediate semiconductor device structure, comprising:
a substrate blank;

at least two semiconductor devices fabricated on the substrate blank, the at least two semiconductor devices positioned adjacent to one another and separated from one another by way of a street extending at least partially across the substrate blank;

at least one through-hole formed substantially through the substrate blank at the street;

a first conductive trace extending from a bond pad of a first semiconductor device of the at least two semiconductor devices to the at least one through-hole; and

a second conductive trace extending from a bond pad of a second semiconductor device of the at least two semiconductor devices to the at least one through-hole.

14. (Withdrawn) The intermediate semiconductor device structure of claim 13, wherein the at least one through-hole has a dimension perpendicular to a direction in which the street extends which exceeds a width of a cut to be made along the street to sever the first and second semiconductor devices from one another.

15. (Withdrawn) The intermediate semiconductor device structure of claim 13, further comprising:

at least one conductive via in the at least one through-hole.

16. (Withdrawn) The intermediate semiconductor device structure of claim 15, wherein the at least one conductive via includes a hollow region extending substantially along a height thereof.

17. (Withdrawn) The intermediate semiconductor device structure of claim 16, wherein the hollow region has a dimension perpendicular to a direction in which the street extends which exceeds a width of a cut to be made along the street to sever the first and second semiconductor devices from one another.

18. (Withdrawn) The intermediate semiconductor device structure of claim 13, further comprising:

an enlargement connecting ends of the first and second conductive traces and surrounding a periphery of an opening of the at least one through-hole.

19. (Withdrawn) The intermediate semiconductor device structure of claim 13, comprising:

a plurality of through-holes located along the street;

a plurality of first conductive traces extending from corresponding bond pads of the first semiconductor device to corresponding through-holes of the plurality of through-holes; and

a plurality of second conductive traces extending from corresponding bond pads of the second semiconductor device to corresponding through-holes of the plurality of through-holes.

20. (Withdrawn) The intermediate semiconductor device structure of claim 13, further comprising:

an insulative layer or structure beneath at least the first conductive trace.

21. (Withdrawn) The intermediate semiconductor device structure of claim 13, further comprising:

an insulative layer covering at least the first conductive trace and the bond pads of the first and second semiconductor devices.

22. (Withdrawn) The intermediate semiconductor device structure of claim 13, further comprising:

a back side insulative layer substantially covering a back side of the substrate blank.

23. (Withdrawn) A semiconductor device assembly, comprising:

a support substrate;

at least one conductive column protruding from the support substrate; and

at least one semiconductor device including an outer connector on a peripheral edge thereof positioned laterally adjacent to and in electrical communication with the at least one conductive column, the outer connector having a height that extends substantially across a height of the peripheral edge.

24. (Withdrawn) The semiconductor device assembly of claim 23, wherein the support substrate comprises at least one of a circuit board, an interposer, leads, and another semiconductor device.

25. (Withdrawn) The semiconductor device assembly of claim 23, wherein the at least one conductive column is in electrical communication with a conductive structure of the support substrate.

26. (Withdrawn) The semiconductor device assembly of claim 25, wherein the at least one conductive column is secured to the conductive structure.

27. (Withdrawn) The semiconductor device assembly of claim 26, wherein at least one of solder, another metal or metal alloy, a conductive elastomer, and a conductor-filled elastomer secures the at least one conductive column to the conductive structure.

28. (Withdrawn) The semiconductor device assembly of claim 25, wherein an end of the at least one conductive column is positioned within an aperture formed in the support substrate, at least a portion of the conductive structure being located adjacent to the aperture.

29. (Withdrawn) The semiconductor device assembly of claim 28, wherein at least the portion of the conductive structure contacts a portion of the end of the at least one conductive column.

30. (Withdrawn) The semiconductor device assembly of claim 28, wherein a quantity of conductive material contacts both the at least one conductive column and the conductive structure.

31. (Withdrawn) The semiconductor device assembly of claim 30, wherein the quantity of conductive material comprises at least one of solder, another metal or metal alloy, a conductive elastomer, and a conductor-filled elastomer.

32. (Withdrawn) The semiconductor device assembly of claim 23, wherein the outer connector of the at least one semiconductor device includes a recess extending substantially along a length thereof.

33. (Withdrawn) The semiconductor device assembly of claim 32, wherein the recess is configured to at least partially receive the at least one conductive column.

34. (Withdrawn) The semiconductor device assembly of claim 23, wherein the at least one conductive column and the outer connector are secured in electrical communication with one another.

35. (Withdrawn) The semiconductor device assembly of claim 34, wherein a quantity of conductive material secures the at least one conductive column and the outer connector in electrical communication with one another.

36. (Withdrawn) The semiconductor device assembly of claim 35, wherein the conductive material comprises at least one of solder, another metal or metal alloy, a conductive elastomer, and a conductor-filled elastomer.

37. (Withdrawn) The semiconductor device assembly of claim 23, comprising a plurality of semiconductor devices in stacked arrangement.

38. (Withdrawn) The semiconductor device assembly of claim 37, wherein adjacent active surfaces and back sides of adjacently positioned semiconductor devices of the plurality of semiconductor devices are substantially electrically isolated from one another.

39. (Withdrawn) The semiconductor device assembly of claim 37, wherein corresponding outer connectors of at least some of the plurality of semiconductor devices are in alignment with one another.

40. (Withdrawn) The semiconductor device assembly of claim 39, wherein aligned outer connectors of the at least some of the plurality of semiconductor devices include recesses therein.

41. (Withdrawn) The semiconductor device assembly of claim 40, wherein the recesses are in-line with one another and at least partially receive the at least one conductive column.

42. (Withdrawn) The semiconductor device assembly of claim 37, wherein the at least one conductive column has a height that is substantially equal to a stack height of the plurality of semiconductor devices.

43. (Withdrawn) The semiconductor device assembly of claim 23, comprising a plurality of conductive columns protruding from the support substrate.

44. (Withdrawn) The semiconductor device assembly of claim 43, wherein each of the plurality of conductive columns is located so as to be positioned adjacent to a single peripheral edge of the at least one semiconductor device.

45. (Withdrawn) The semiconductor device assembly of claim 43, wherein the plurality of conductive columns are located so as to be positioned adjacent to more than one peripheral edge of the at least one semiconductor device.

46. (Withdrawn) A support element for supporting at least one semiconductor device, comprising:

a support substrate including at least one conductive structure thereon; and

at least one conductive column protruding from the support substrate and in communication with the at least one conductive structure, the at least one conductive column being configured to contact an outer connector on a peripheral edge of the at least one semiconductor device.

47. (Withdrawn) The support element of claim 46, wherein the at least one conductive column comprises a wire comprising conductive material.

48. (Withdrawn) The support element of claim 47, wherein the wire comprises at least one of gold, copper, and aluminum.

49. (Withdrawn) The support element of claim 46, wherein a cross-section of the at least one conductive column, taken transverse to a length thereof, has a semicircular shape.

50. (Withdrawn) The support element of claim 46, wherein an end of the at least one conductive column is at least partially supported within an aperture formed in the support substrate.

51. (Withdrawn) The support element of claim 46, comprising a plurality of conductive columns in communication with a corresponding plurality of conductive structures of the support substrate.

52. (Withdrawn) The support element of claim 46, wherein the support substrate comprises at least one of a circuit board, an interposer, leads, and another semiconductor device.